Patent abstract files

0014893382 *Drawing available*
WPI Acc no: 2005-241125/200525 your application
XRPX Acc No: N2005-198749
Message e.g. edit and create message, persistence enhancing method, involves copying message to working queue to persist message before message is removed from inbound queue, and processing message to generate reply
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: PHILLIPS B R

Patent Family (1 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050060374	A1	20050317	US 2003660289	A	20030911	200525	B

Priority Applications (no., kind, date): US 2003660289 A 20030911

Alerting Abstract US A1
NOVELTY - The method involves browsing an **inbound queue** (135) to identify a **message**. The **message** is **copied** to a **working queue** to persist the message before the message is removed from the **inbound queue**, where the **working queue** is persisted by a queue manager. The message is locked until the **message** is **copied** to the **working queue**. The **message** is processed to generate a reply prior to removing the message from the **working queue**.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

a. an apparatus for enhancing persistence of a message
b. a machine-accessible medium containing instructions.

USE - Used for enhancing persistence of a message e.g. an edit and create message, that is communicated between computer systems e.g. workstation, server, mobile computer and personal digital assistant, of a local area network or wide area network.
ADVANTAGE - The method enhances persistence of the message to greatly avoid loss of the message after receipt, thus improving the network performance.
DESCRIPTION OF DRAWINGS - The drawing shows a system for enhancing persistence of a message.
130Server
132Acceptor
135Inbound queue
140Dispatcher
142Thread pool

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
G06F-0015/16	A	I		R	20060101
G06F-0015/16	C	I		R	20060101

ECLA: G06F-009/46R6M
US Classification, Current Main: 709-206000
US Classification, Issued: 709206
Manual Codes (EPI/S-X): T01-F02A; T01-N02A2; T01-S03

12/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0008567248 *Drawing available*
WPI Acc no: 1998-101242/199809
XRPX Acc No: N1998-081090
Access system for distributed storage - delivers units of code or data to search interface, and uses management interfaces between submission and search interfaces to provide categorisation
Patent Assignee: BRITISH TELECOM PLC (BRTE)
Inventor: CORLEY S L; HAYES E J P; REED J W; SHORTLAND R J; WHITTLE B R

Patent Family (7 patents, 75 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1998001809	A1	19980115	WO 1997GB1828	A	19970708	199809	B
AU 199734520	A	19980202	AU 199734520	A	19970708	199826	E
EP 910828	A1	19990428	EP 1997930640	A	19970708	199921	E
			WO 1997GB1828	A	19970708		
JP 2000514225	W	20001024	WO 1997GB1828	A	19970708	200058	E
			JP 1998504940	A	19970708		
EP 910828	B1	20010926	EP 1997930640	A	19970708	200157	E
			WO 1997GB1828	A	19970708		
US 6304874	B1	20011016	WO 1997GB1828	A	19970708	200164	E
			US 199891948	A	19980626		
DE 69706987	E	20011031	DE 69706987	A	19970708	200173	E
			EP 1997930640	A	19970708		

			WO 1997GB1828	A	19970708

Priority Applications (no., kind, date): EP 1996305063 A 19960709

Alerting Abstract WO A1
The broking system for software or data receives submission inputs which are made to a warehousing database, each of which comprises a descriptive data set in relation to a unit of data or software, together with an address field (32). The broking system (13) loads the submission input to the warehousing database, and it to temporary data stores identified in the address field.
Each temporary data store is allocated to a respective management interface (12) and is viewable to that management interface (12) only. Inputs can be made at the management interface (12) to transfer the descriptive data sets received to an index accessible by a number of search interfaces (11), or to delete the descriptive data set from the temporary data store.
USE - Accessing units of data or software in distributed storage, for re-use of software units in e.g. building of standardised strategic architectures, e.g. building operating support systems in telecommunications environment.
ADVANTAGE - Provides flexibility and scalability in distributed 'library' while maintaining simple access capability.

Class Codes

International Patent Classification					
IPC	**Class Level**	**Scope**	**Position**	**Status**	**Version Date**
G06F-017/30			Main		"Version 7"
G06F-0017/30	A	I		R	20060101
G06F-0017/30	C	I		R	20060101

ECLA: G06F-017/30N
US Classification, Issued: 70710, 7072
File Segment: EPI;
DWPI Class: T01
Manual Codes (EPI/S-X): T01-J05B4A; T01-J20B2

Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**unit of data or software, together with an address field (32). The broking system (13) loads the submission input to the warehousing database (20) and **copies** it to **temporary data stores** (32) **identified in the** address field. Each **temporary** data **store** (32) **is** allocated **to** a respective management interface (12) and is viewable to that management interface (12) only. Inputs can be made at the management interface (12) to transfer... ... or software, together with an address field (32). The broking system (13) loads the submission input to the warehousing database (20) and copies it to **temporary data stores** (32) identified in **the** address field. **Each temporary data store** (32) is allocated to a respective **management** interface (**12**) and is viewable to that management

interface (12) only. Inputs can be made at the management interface (12) to transfer the descriptive data sets received... ...**Claims:**the distributed storage; (ii) a set of indexes for containing respective lists of descriptive data sets selected from the descriptive data sets which have been **input** to the database; **and** (iii) control means for controlling the contents of the set of indexes; wherein each index has associated with it a data store to which selected d...

18/69,K/1 (Item 1 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0010372786 *Drawing available*
WPI Acc no: 2000-025244/200003
XRPX Acc No: N2000-018908
Improved buffering arrangement in receiver and decoder solving difficulty of maintaining and updating both icons and titles satisfactorily, particularly as title can appear at any screen position
Patent Assignee: THOMSON LICENSING SA (CSFC); CANAL& (CANA-N); CANAL+ SA (CANA-N); CANAL+ TECHNOLOGIES (CANA-N)
Inventor: LETOURNEUR P; MERIC J

Patent Family (21 patents, 85 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 954171	A1	19991103	EP 1998401075	A	19980429	200003	B
WO 1999056465	A1	19991104	WO 1999IB850	A	19990429	200003	E
AU 199936224	A	19991116	AU 199936224	A	19990429	200015	E
BR 199910053	A	20010109	BR 199910053	A	19990429	200106	E
			WO 1999IB850	A	19990429		
NO 200005403	A	20001222	NO 20005403	A	20001026	200106	E
			WO 1999IB850	A	19990429		
EP 1078515	A1	20010228	EP 1999918203	A	19990429	200113	E
			WO 1999IB850	A	19990429		
CZ 200003997	A3	20010613	CZ 20003997	A	19990429	200138	E
			WO 1999IB850	A	19990429		
KR 2001043114	A	20010525	KR 2000712003	A	20001028	200168	E
CN 1307780	A	20010808	CN 1999808026	A	19990429	200173	E
ZA 200006804	A	20011031	ZA 20006804	A	20001121	200173	E
HU 200102700	A2	20011128	HU 20012700	A	19990429	200209	E
			WO 1999IB850	A	19990429		
MX 2000010628	A1	20010501	MX 200010628	A	20001027	200227	E

JP 2002513253	W	20020508	JP 2000546517	A	19990429	200234	E
			WO 1999IB850	A	19990429		
NZ 507809	A	20020426	NZ 507809	A	19990429	200236	E
			WO 1999IB850	A	19990429		
EP 1078515	B1	20021002	EP 1999918203	A	19990429	200272	E
			WO 1999IB850	A	19990429		
DE 69903281	E	20021107	DE 69903281	A	19990429	200281	E
			EP 1999918203	A	19990429		
			WO 1999IB850	A	19990429		
ES 2184444	T3	20030401	EP 1999918203	A	19990429	200328	E
MX 223503	B	20041015	MX 200010628	A	20001027	200557	E
			WO 1999IB850	A	19990429		
KR 613220	B1	20060818	KR 2000712003	A	20001028	200714	E
			WO 1999IB850	A	19990429		
US 7284262	B1	20071016	US 2000674079	A	20001025	200768	E
			WO 1999IB850	A	19990429		
CN 100399811	C	20080702	CN 1999808026	A	19990429	200864	E

Priority Applications (no., kind, date): EP 1998401075 A 19980429

Alerting Abstract EP A1

NOVELTY - Arrangement divides the data buffer area (45A) into two subareas with incoming data directed into one of them as directed by control circuitry. The two subareas can be interchanged so that further incoming display data is stored in the other subarea and graphics data stored in a graphics buffer area is passed to the other subarea. The graphics area (45) may be divided into several subareas.

USE - For providing a method for processing data.

ADVANTAGE - Maintains and updates both icons and titles satisfactorily, particularly as title can appear at any screen position.

DESCRIPTION OF DRAWINGS - The drawing shows a schematic diagram of the RAM memory graphics processor.

45A the data buffer area

45 the graphics buffer area

Class Codes

International Patent Classification					
IPC	**Class Level**	**Scope**	**Position**	**Status**	**Version Date**
G09G-001/16; H04N; H04N-005/445			Main		"Version 7"

G09G-0001/16	A	I	L	B	20060101		
G09G-0001/16	A	I		R	20060101		
G09G-0005/00	A	I	L	R	20060101		
G09G-0005/395	A	I		R	20060101		
G09G-0005/399	A	I		R	20060101		
H04N-0005/445	A	I	F	B	20060101		
H04N-0005/445	A	I		R	20060101		
H04N-0007/16	A	I	L	B	20060101		
H04N-0007/173	A	I	L	B	20060101		
H04N-0009/64	A	I	F	B	20060101		
G09G-0001/16	C	I	L	B	20060101		
G09G-0001/16	C	I		R	20060101		
G09G-0005/00	C	I	L	R	20060101		
G09G-0005/36	C	I		R	20060101		
H04N-0005/445	C	I	F	B	20060101		
H04N-0005/445	C	I		R	20060101		
H04N-0007/16	C	I	L	B	20060101		
H04N-0007/173	C	I	L	B	20060101		
H04N-0009/64	C	I	F	B	20060101		

ECLA: G09G-005/395, G09G-005/399, H04N-005/445
US Classification, Current Main: 725-142000; Secondary: 348-714000, 348-715000, 348-716000, 348-718000 , 725-134000
US Classification, Issued: 725142, 348714, 348715, 348716, 348718, 725134

Manual Codes (EPI/S-X): T01-C07C2; T01-D02; T01-J10C; T01-J12D

Original Publication Data by AuthorityArgentina**Publication No. ...Original Abstracts:**method of processing video data in a receiver/decoder comprising at least one port (31) for receiving data and memory means (40) comprising a data **buffer** area (45A0, 45A1) for storing **incoming** data for display, and a graphics buffer area (45Ai) for storing graphics data, said method comprising passing graphics data stored in the graphics buffer area... ... method of processing video data in a receiver/decoder comprising at least one port 31 for receiving data and memory means 40 comprising a data **buffer** area 45A0, 45A1 for storing **incoming** data for display, and a graphics buffer area 45Ai for storing graphics data, said method comprising passing graphics data stored in the graphics buffer area... ... method of processing video data in a receiver/decoder including at least one port (**31**) for receiving data and memory means (**40**) including a data **buffer** area (**45**A0**, 45**A1) for storing **incoming** data for display, and a graphics buffer area (**45**Ai) for storing graphics data, said method including passing graphics data

stored in the graphics buffer area... ... method of processing video data in a receiver/decoder comprising at least one port (31) for receiving data and memory means (40) comprising a data **buffer** area (45A0, 45A1) for storing **incoming** data for display, and a graphics buffer area (45Ai) for storing graphics data, said method comprising passing graphics data stored in the graphics buffer area... ...**Claims:**A method of processing video data in a receiver/decoder comprising at least one port for receiving data and memory means comprising a data **buffer** area for storing **incoming** data for display, and a graphics buffer area for storing graphics data, said method comprising passing graphics data stored in the graphics buffer area to... ... 1. A method of processing video data in a receiver/decoder comprising at least one port for receiving data and memory means comprising a data **buffer** area for storing **incoming** data for display, and a graphics buffer area for storing graphics data, said method comprising passing graphics data stored in the graphics buffer area to... ... decoder comprising:designating a first buffer sub-area as a display buffer;designating a second buffer sub-area as a working buffer, wherein the working **buffer** is initially reserved only for **incoming** subtitle data comprising at least one subtitle, and wherein a content of the **working** buffer is constantly changing;storing subtitle data in the **working buffer** to obtain a complete subtitle page;storing graphics data in a third buffer sub-area; and**copying** the graphics **data** from the third buffer sub-area into the **working buffer** after obtaining the complete subtitle page to obtain a complete image;interchanging roles of the **working buffer** and the display buffer such that the complete image is transferred from the **working buffer** to the display buffer; anddisplaying the complete subtitle page,wherein the graphics **data** is **copied** into the **working buffer** just before the **working buffer** becomes the display buffer,wherein the complete image comprises both the complete subtitle page and the graphics data, andwherein the first buffer sub-area...

18/69,K/2 (Item 2 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0007922009 *Drawing available*
WPI Acc no: 1997-009764/199701
XRPX Acc No: N1997-008960
Packet switching appts. with multiplexer-demultiplexer for integrated services digital network - has system clock distribution unit which supplies system clock to each unit which inputs external system clock
Patent Assignee: ELECTRONICS & TELECOM RES INST (ELTE-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N); KOREA TELECOM AUTHORITY (KOTE-N); KOREA TELECOM CORP (KOTE-N); KOREA TELECOM MUNITION AUTHORITY (KOTE-N)
Inventor: KIM H; KIM H J; KIM K; KIM K B; KIM K S; LEE J; LEE J J

Patent Family (4 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 8280080	A	19961022	JP 1995329333	A	19951218	199701	B
US 5732085	A	19980324	US 1995573093	A	19951215	199819	E

KR 126848	B1	19980401	KR 199434756	A	19941216	200009	E
JP 3151139	B2	20010403	JP 1995329333	A	19951218	200121	E

Priority Applications (no., kind, date): KR 199434756 A 19941216

Alerting Abstract JP A

The appts. has input port drive units (31) which execute a connection function between adjacent units. The data applicable to a packet flow and a continuous packet with control signal, are input to the IPDU. A demultiplexing and a reproduction are performed on the packet based on a target point data signal. Several switch input demultiplexer units (32) execute the function of temporarily storing the packet during overflow in a specific input link. Each packet routed to each SIDU through an interactive **input** link, is **input** to a **buffer** and output as the packet flow. Several switching output multiplexer units perform multiplexing on the collected packet.

Several output port drive units output the packet flow through each interface. A switch module control unit inspects and controls each SOMU condition and transmits the inspection result to a processor. A switch change over controller executes the change over function mistaken according to the condition data on SMCU, and substitutes a generation switch. A system clock distribution unit supplies a system clock to each unit that inputs external system clock.

ADVANTAGE - Prevents switching trouble due to temporary overflow.

Class Codes

International Patent Classification					
IPC	**Class Level**	**Scope**	**Position**	**Status**	**Version Date**
H04J-0003/24	A	I		R	20060101
H04L-0012/56	A	I		R	20060101
H04Q-0011/04	A	I	F	R	20060101
H04J-0003/24	C	I		R	20060101
H04L-0012/56	C	I		R	20060101
H04Q-0011/04	C	I	F	R	20060101

ECLA: H04J-003/24D, H04L-012/56S1A
ICO: T04L-012:56A20, T04L-012:56A2B1, T04L-012:56A2G
US Classification, Issued: 370398, 370395, 370413, 370218
Manual Codes (EPI/S-X): W01-A03B; W01-A06A; W01-A06G2

Alerting Abstract ...32) execute the function of temporarily storing the packet during overflow in a specific input link. Each packet routed to each SIDU through an interactive **input** link, is **input** to a **buffer** and output as the packet flow. Several switching output multiplexer units perform multiplexing on the collected packet... Original Publication Data by AuthorityArgentina**Publication No.** ...**Original Abstracts:**traffic phenomenon of one output port in the switching apparatus, reduce the necessary buffer according to

the effect of the rate gain and process smoothly **input** traffic of the **internal buffer** having a burst **characteristic**. Further more, the present invention has a duplicate function of cells able to provide a broadcast-type service distributed to subscribers at one time so... ...**Claims:**a packet flow and a packet flow-related control signal from the IPDU, judging the selecting or non-selecting of the packets, temporarily storing the **packets**, demultiplexing **and duplicating** the **packets for** routing the **packet** according **to** the target point **information** signal and performing a **temporary store** function of the packets **when an** overflow occurs on a specific input link; a plurality of switching output multiplexer units (SOMU) for inputting and collecting in an output buffer each of the packets routed through the **input** links fully interconnected with the respective SIDU and multiplexing the collected packets for outputs as a packet flow; a plurality of output port driving units...

18/69,K/3 (Item 3 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0006794041 *Drawing available*
WPI Acc no: 1994-180316/199422
XRPX Acc No: N1994-142274; N1995-127116
Shared-buffer-type ATM switch with improved circuit throughput - uses broadcast function with exclusive output to broadcast cells to avoid undesirable wait time
Patent Assignee: HITACHI LTD (HITA)
Inventor: AIKI K; ENDO N; KOZAKI T; OZAKI N; SHIBATA H; SHIBATA J

Patent Family (3 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
JP 6120974	A	19940428	JP 1992269969	A	19921008	199422	B
US 5410540	A	19950425	US 1993132999	A	19931007	199522	ETAB
JP 3104429	B2	20001030	JP 1992269969	A	19921008	200057	E

Priority Applications (no., kind, date): JP 1992269969 A 19921008

Alerting Abstract US A
The shared-buffer-type ATM switch includes a multiplexer for multiplexing ATM cells input from ports. The resulting multiplexed ATM cells are stored in a shared buffer memory section. A buffer memory control section is used for writing and reading the ATM cells into and from the shared buffer memory section.A demultiplexer for use with the multiplexed ATM cells,
transmits the demultiplexed ATM cells to output ports. A cell copy section, located between the multiplexer and the shared buffer memory section, produces copies of a broadcast cell.
The cell copy section includes a copy FIFO buffer which is used for **temporary storage** of the ATM cells and a **copy information** table for storing routing **information** and **copy** count **information**. A routing **information** adding unit is coupled to the **copy** FIFO

buffer and adds routing **information** to the ATM cells output from the copy FIFO buffer. A copy controller is also coupled to the copy FIFO buffer, and uses the copy information table and routing information adding unit to copy an ATM cell. A broadcast cell can also be copied but routing information associated with an outport port is also added to each copied cell and the cell is read in memory. In response to an output counter, the cell is read from memory and broadcast to an output port.
USE/ADVANTAGE - Output port designating cycle for broadcast cell unnecessary. Suppression of wait state of output cells.

Class Codes

International Patent Classification

IPC	Class Level	Scope	Position	Status	Version Date
H04L-0012/18	A	I		R	20060101
H04L-0012/56	A	I		R	20060101
H04Q-0011/04	A	I	L	R	20060101
H04Q-0003/52	A	I	F	R	20060101
H04L-0012/18	C	I		R	20060101
H04L-0012/56	C	I		R	20060101
H04Q-0011/04	C	I	L	R	20060101
H04Q-0003/52	C	I	F	R	20060101

ECLA: H04L-012/18, H04L-012/56S1C
ICO: T04L-012:56A2B3, T04L-012:56A2D
US Classification, Issued: 37060, 37061
Manual Codes (EPI/S-X): W01-A03B1; W01-A06G2

Alerting Abstract ...The cell copy section includes a copy FIFO buffer which is used for **temporary storage** of the ATM cells and a **copy information** table for storing routing **information** and **copy** count **information**. A routing **information** adding unit is coupled to the **copy** FIFO buffer and adds routing **information** to the ATM cells output from the copy FIFO buffer. A copy controller is also coupled to the copy FIFO buffer, and uses the copy ... Original Publication Data by AuthorityArgentina**Publication No. Claims:**A shared-buffer-type ATM switch comprising: a multiplexer for multiplexing ATM cells inputted from a plurality of input ports **and** outputting multiplexed cells; a shared **buffer** for storing therein the multiplexed cells; a demultiplexer for demultiplexing cells read out from the shared buffer and sending demultiplexed cells to output ports; a cell copy section provided between an output of said multiplexer and an **input** of **said** shared **buffer** for **producing** a predetermined number of copies of a broadcasting cell from said multiplexer and storing copied cells in said shared buffer; and a buffer control section...

Patent full-text files

12/5K/2 (Item 1 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

01231475

EQUIPMENT COMPONENT MONITORING AND REPLACEMENT MANAGEMENT SYSTEM

Patent Applicant/Patent Assignee:

- **HYDRALIFT AMCLYDE INC**
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Patent Applicant/Inventor:

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- **BOOTH Michael L**
  4232 Monroe Street, Columbia Heights, MN 55421; US; US(Residence); US(Nationality); (Designated only for: US)
- **WALLER Aaron D**
  811 8th Street, Apt. 22, Farmington, MN 55024; US; US(Residence); US(Nationality); (Designated only for: US)
- **HOLME Anders**
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- **FRAFJORD Erik**
  Kloverveien 20, N-4050 Sola; NO; NO(Residence); NO(Nationality); (Designated only for: US)
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  14/41 Queensgate Terrace, London SW7 MPN; NO; GB(Residence); NO(Nationality); (Designated only for: US)

Legal Representative:

- **HEMPHILL Stuart R(et al)(agent)**
  Dorsey & Whitney LLP, Intellectual Property Department, Suite 1500, 50 South Sixth Street, Minneapolis, MN 54402-1498; US;

	Country	Number	Kind	Date
Patent	WO	200538613	A2-A3	20050428
Application	WO	2004US34016		20041014
Priorities	US	2003512108		20031017
	US	2004567705		20040503

Main International Patent Classes (Version 7):

IPC	Level
G06F-017/60	Main

Language Publication Language: English
Filing Language: English
Fulltext word count: 18679

English Abstract:

A system for managing replacement components for equipment (300, 400) having a plurality of components each with a limited useful life has a computer (40) with a processor (100). The system includes a computer program module for defining a duty profile (220) comprising a plurality of usage cases for the equipment (300, 400), each usage case involving two or more of the plurality of components and specified operating conditions assumed to be experienced by the involved components during the execution of each of the usage cases. There are also a computer program module for determining a theoretical useful life for each component involved in a duty profile (220), the theoretical useful life being based on component useful life data under the specified operating conditions; and sensors (302, 402) for determining and monitoring the occurrence of equipment operation corresponding to a usage case.

French Abstract:

L'invention concerne un systeme pour gerer des composants de remplacement pour un equipement representant une pluralite de composants. Chaque composant presentant une vie utile limitee possede un ordinateur dote d'un processeur. Le systeme comprend un module de programme informatique pour definir un profil de travail comprenant une pluralite de cas d'usage de l'equipement. Chaque cas d'usage implique au moins deux composants et des conditions de fonctionnement specifiees supposement associees aux composants en question, lors de l'execution de chaque cas d'usage. L'invention concerne egalement un module de programme informatique pour determiner une vie utile theorique pour chaque composant implique dans un profil de travail. Cette vie utile theorique est fondee sur des donnees de vie utile de composant, dans des conditions de fonctionnement specifiees ; et des capteurs pour determiner et pour surveiller l'apparition d'un fonctionnement d'equipement correspondant a un cas d'usage, et pour mesurer les conditions de fonctionnement reelles dans son mode de fonctionnement et dans un certain nombre d'autres modes de fonctionnement. L'invention concerne un module de

programme informatique different permettant de calculer une vie utile theorique reglee pour un composant fonctionnant dans au moins un mode de fonctionnement, en fonction d'une comparaison des conditions de fonctionnement reelles et des conditions de fonctionnement supposees lors d'un fonctionnement correspondant a un cas d'usage.

Detailed Description:

...flow during the monitoring of the equipment will be explained. In addition to the elements shown in FIG. 12, FIG. 13 also shows an outbound **queue** 92 and an **inbound queue** 90 as well as an FTP ffile transfer protocol) server 91 and a network interface 93.

[0134] The measurement data from the on-site computer 64 is received through the network interface 93 by the FTP server 91. The data is put in the **inbound queue** 90. The logstream handler 80 is configured to get data from the **inbound queue** 90 at regular intervals.

In the logstream handler 80 the data are arranged so that these are presented in an order that will enable **temporary storage** in the measurement database 82. The function of the logstrearn handler 80 will be explained in more detail below.

[0135] A **copy** of the **data** transmitted to the measurement database 82 is also stored in the bulk storage 85. The purpose of this is, firstly, for backup and, secondly, to...

00871545

File system level compression using holes
Compression de niveaux avec des trous dans un systeme de fichiers

Patent Assignee:

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	Country	Number	Kind	Date
Patent	EP	798656	A2	19971001 (Basic)
	EP	798656	A3	19990818
	EP	798656	B1	20030122
Application	EP	97301739		19970314
Priorities	US	623907		19960327

International Patent Class (V7): G06F-017/30

CITED PATENTS: (EP B)

EP 587437 A; US 5280600 A; US 5305295 A;

Abstract EP 798656 A2

A method, apparatus, and computer-usable medium for compressing data in a file system utilizing the concept of "holes". A mapping table in a file system maps the logical blocks of a file to actual physical blocks on disk where the data is stored. Blocks may be arranged in units of a cluster, and the file may be compressed cluster-by-cluster. Holes are used within a cluster to indicate not only that a cluster has been compressed, but also the compression algorithm used. Different clusters within a file may be compressed with different compression algorithms. A unit of data is compressed, with the result that the file occupies fewer physical blocks than it has logical blocks. The mapping table is updated to indicate that for a given unit of data compressed, fewer physical blocks are needed. Certain logical blocks belonging to this unit of data are not mapped to physical blocks but are mapped to a hole. A hole indicates that the unit of data was compressed, and may also indicate the particular compression algorithm used to compress the unit of data. If a unit of data begins or ends within the middle of a cluster, to avoid overwriting the data not to be changed the whole cluster must first be read from disk. If a hole indicates the cluster had been compressed, the data must be expanded first. The cluster is read into a buffer and the portion to be changed is overwritten. The cluster is compressed and written back to disk. Those clusters within which the unit of data neither begins nor ends may be written to directly.

Specification: ...807 to 811. Steps 807 to 813 which are used when a full cluster is not being written describe a situation in which either the **Input Buffer** begins at an intermediate location within a cluster or ends at an intermediate location within a cluster. If the **Input Buffer** begins at the beginning of a cluster and ends at the end of a cluster then these steps are not needed. The following variables are used in the steps 807 to 813:

Cluster Number is the cluster at which the data will be retrieved, Read Buffer is a **temporary** data buffer that will contain the data to be retrieved, Cluster Offset is the offset within the Read **Buffer** at which data from the **Input Buffer** will be copied to, **Input Buffer** contains the **data** to be written, and **Input Buffer** Offset is a location within the **Input Buffer** from which the data will be written to disk.

In step 807 the Read Buffer is cleared by setting all bytes in the Read Buffer... ...stored in the Read Buffer. This step 809 will be explained more fully below with reference to Figure 7. In step 811 data from the **Input Buffer** is copied to the Read Buffer. This step may be performed by copying Write Size bytes of data from the location at the Input Buffer...

Specification: ...807 to 811. Steps 807 to 813 which are used when a full cluster is not being written describe a situation in which either the **Input Buffer** begins at an intermediate location within a cluster or ends at an intermediate location within a cluster. If the **Input Buffer** begins at the beginning of a cluster and ends at the end of a cluster then these steps are not needed. The following variables are used in the steps 807 to 813: Cluster Number is the cluster at which the data will be retrieved, Read Buffer is a **temporary** data buffer that will contain the data to be retrieved, Cluster Offset is the offset within the Read **Buffer** at which data from the **Input Buffer** will be copied to, **Input Buffer** contains the **data** to be written, and **Input Buffer** Offset is a location within the **Input Buffer** from which the data will be written to disk.

In step 807 the Read Buffer is cleared by setting all bytes in the Read Buffer... ...stored in the Read Buffer. This step 809 will be explained more fully below with reference to Figure 7. In step 811 data from the **Input Buffer** is copied to the Read Buffer. This step may be performed by copying Write Size bytes of data from the location at the Input Buffer...

18/5K/2 (Item 2 from file: 348)
DIALOG(R)File 348: EUROPEAN PATENTS

00564638

Programmable hand held labeler
Etiqueteuse manuelle programmable

Patent Assignee:

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	Country	Number	Kind	Date	
Patent	EP	571734	A1	19931201	(Basic)
	EP	571734	B1	19960424	
Application	EP	93104667		19930322	
Priorities	US	858703		19920327	

International Patent Class (V7): B65C-011/02; ;

CITED PATENTS: (EP A)

EP 430609 A; EP 430609 A; US 4652317 A; EP 209752 A; EP 208203 A;

Abstract EP 571734 A1

A hand held labeler is programmable to operate in accordance with a sequence of commands forming an application program that is downloaded to the labeler and stored in a random access memory. Each command is associated with a command routine selected from a set of command routines that is stored in a read only memory. The commands of the application program and associated command routines are executed by a microprocessor of the labeler to perform flexible data collection, data manipulation and label printing operations. (see image in original document)

Specification: ...work buffer 126 can be copied to the look up table work buffer 120, the data collect file 132, the header work buffer 122, the **temporary** work **buffer** 118 and/or the print buffer 124. The data in the header work buffer 122 can be **copied** to the **data**

collect file 132, the look up table work buffer 120, the data collect work buffer 126, the **temporary** work **buffer** 118 and/or the print buffer 124. Further, data in the temporary work buffer can be copied to the look up table work buffer 120... ...buffer 126, the header work buffer 122 and/or the print buffer 124. It is noted that the print buffer 124 is a write only **buffer**.

The data **input** to the labeler 10 is manipulated and moved among the various work buffers and files to associate selected data together in a flexible manner so...be stripped, the number being any number from 1 to 64. The first field specified in the Strip command may be a field in the **input buffer** 133, the temporary work **buffer** 118, the data collect work buffer 126, the look up table work buffer 120 or the header work buffer 122. The second field may be... ...get at a block 930 the number of characters to be stripped as specified in the command. Thereafter, the microprocessor 110 at a block 931 **copies** the **data** in the specified first field to the **temporary** work **buffer** 118. At a block 932 the microprocessor 110 determines whether the characters are to be stripped from the right and if not, the microprocessor proceeds...

Specification: ...work buffer 126 can be copied to the look up table work buffer 120, the data collect file 132, the header work buffer 122, the **temporary** work **buffer** 118 and/or the print buffer 124. The data in the header work buffer 122 can be **copied** to the **data** collect file 132, the look up table work buffer 120, the data collect work buffer 126, the **temporary** work **buffer** 118 and/or the print buffer 124. Further, data in the temporary work buffer can be copied to the look up table work buffer 120... ...buffer 126, the header work buffer 122 and/or the print buffer 124. It is noted that the print buffer 124 is a write only **buffer**.

The data **input** to the labeler 10 is manipulated and moved among the various work buffers and files to associate selected data together in a flexible manner so...be stripped, the number being any number from 1 to 64. The first field specified in the Strip command may be a field in the **input buffer** 133, the temporary work **buffer** 118, the data collect work buffer 126, the look up table work buffer 120 or the header work buffer 122. The second field may be... ...get at a block 930 the number of characters to be stripped as specified in the command. Thereafter, the microprocessor 110 at a block 931 **copies** the **data** in the specified first field to the **temporary** work **buffer** 118. At a block 932 the microprocessor 110 determines whether the characters are to be stripped from the right and if not, the microprocessor proceeds...

18/5K/4 (Item 1 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

01608466

EFFICIENTLY POLLING TO DETERMINE COMPLETION OF A DMA COPY OPERATION

INTERROGATION EFFICACE POUR DETERMINER L'ACHEVEMENT D'UNE OPERATION DE COPIE DMA

Patent Applicant/Patent Assignee:

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Inventor(s):

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  c/o Microsoft Corporation$International Patents$One Microsoft Way$Redmond, Washington 98052-6399; US; (Designated for all)

	Country	Number	Kind	Date
Patent	WO	200805105	A1	20080110
Application	WO	2007US11633		20070514
Priorities	US	2006479907		20060630

International Patent Classes (Version 8/R)

IPC	Level	Value	Position	Status	Version	Action	Source	Office
H04L-0012/56	A	I	F	B	20060101		H	KR
G06F-0012/16	A	I	L	B	20060101		H	KR

Language Publication Language: English
Filing Language: English
Fulltext word count: 10839

English Abstract:

Efficiently polling a DMA module to determine if the DMA copying of a packet payload to an application buffer is complete. For communication packets received from a network, a processing module may be configured to poll the DMA module at times when it is likely that the DMA copying of packet payloads is complete. Packets may be received and processed in batches. The polling of the DMA module for a packet belonging to a first batch may be deferred until the processing of a next batch. An exception may occur if a predefined amount of time elapses following the completion of

the processing of the first batch before the next batch is received. In response to the predefined amount of time elapsing before the receipt of the next batch, the DMA module may be polled, i.e., prior to the next batch being processed.

French Abstract:

L'interrogation efficace d'un module DMA consiste a determiner si la copie DMA de donnees utiles de paquet vers un tampon d'application est terminee. Pour les paquets de communication recus d'un reseau, un module de traitement peut etre configure pour interroger le module DMA au moment ou la copie DMA de donnees utiles de paquets devrait etre terminee. Les paquets peuvent etre recus et traites par lots. L'interrogation du module DMA concernant un paquet appartenant a un premier lot peut etre differee jusqu'au traitement d'un lot suivant. Il peut se produire une exception s'il s'ecoule un temps predefini suite a l'achevement du traitement du premier lot avant reception du lot suivant. En reponse au temps predefini s'ecoulant avant la reception du lot suivant, le module DMA peut etre interroge, a savoir, avant le traitement du lot suivant.

Detailed Description:

...entire TCP connection to the hardware; "Remote DMA" (RDMA), which makes it possible for a NIC to employ direct memory access (DMA) techniques to send **incoming** packets directly to the application **buffer** (without CPU assistance); and "Receive Side Scaling" (RSS), which distributes the processing of receive packets across multiple processors.

One of the most CPU-intensive tasks during receive processing (i.e., the processing of packets received from a network) is copying an **incoming** packet from a NIC receive **buffer** to an application buffer. This copy results from the following process. At the time of receiving a network packet, NIC hardware does not know the final destination of the **packet** payload. Therefore, the hardware **copies** the **packet** to a **temporary buffer** (i.e., a NIC receive buffer). After TCP/IP processing of the packet identifies the application buffer (I/O request buffer) to which the **packet** payload should be **copied**, the CPU is utilized to copy the payload to the application buffer. A DMA engine can be used to perform this copy without CPU intervention...

18/5K/5 (Item 2 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT
 Bad date

01397986

LAYERED MULTICAST AND FAIR BANDWIDTH ALLOCATION AND PACKET PRIORITIZATION
MULTI-DIFFUSION EN COUCHES ET ATTRIBUTION EXACTE DE LARGEUR DE BANDE ET PRIORISATION DE PAQUETS

Patent Applicant/Patent Assignee:

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Patent Applicant/Inventor:

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Legal Representative:

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	Country	Number	Kind	Date
Patent	WO	200681454	A2-A3	20060803
Application	WO	2006US2995		20060126
Priorities	US	2005647601		20050126

International Patent Classes (Version 8/R)

IPC	Level	Value	Position	Status	Version	Action	Source	Office
H04L-0012/28	A	I	F	B	20060101		H	US

Language Publication Language: English
Filing Language: English
Fulltext word count: 22435

English Abstract:

Embodiments include an overlay multicast network. The overlay multicast network may provide a set of features to ensure reliable and timely arrival of multicast data. The embodiments include a congestion control system that may prioritize designated layers of data within a data stream over other layers of the same data stream. Each data stream transmitted over the network may be given an equal share of the bandwidth. Addressing in routing tables maintained by routers in the may utilize summarized addressing based on the difference in location of the router and destination address. Summarization levels may be adjusted to minimize travel distances for packets in the network. Data from high

priority data stream layers may also be retransmitted upon request from a destination machine to ensure delivery of data.

French Abstract:

Des modes de realisation de cette invention concernent un reseau superpose de multi-diffusion. Ledit reseau peut engendrer une serie de caracteristiques de maniere a garantir une arrivee fiable et ponctuelle des donnees de mutli-diffusion. Certains modes de realisation ont pour objet un systeme de regulation de l'encombrement qui peut mettre en priorite des couches designees de donnees au sein d'un flux de donnees parmi d'autres couches du meme flux de donnees. Chaque flux de donnees transmis par le reseau peut se voir attribuer une part egale de la largeur de bande. L'adressage dans des tableaux de routage maintenus par des routeurs utilise un adressage abrege en fonction de la difference d'emplacement du routeur et de l'adresse de destination. Des niveaux d'abregement peuvent etre ajustes de maniere a minimiser des distances de trajet de paquets dans le reseau. Des donnees provenant de couches de flux de donnees de priorite elevee peuvent etre, egalement, transmises suite a une demande emanant d'une machine destinataire afin d'assurer la distribution de donnees.

Detailed Description:

...the present example, the packets are passed to the first outbound interceptor (PRI) of the interface (path 2). The PRI is responsible for storing a **copy** of each recoverable **packet** that is transmitted. It stores the **copies** in the private **temporary packet store** 915 of its interface (path 3). Then the interceptor passes the packets to the next interceptor (CCI) (path 4) where it is buffered until the... ...and sent through that router's inbound interceptor pipeline 921 (path 7). They first enter the PRI 923 (path 7), which stores copies in its **inbound buffer** 924 (path 8) and then passes them on to the next interceptor (CCI) 925 (path 9) where they are temporarily parked until the router's...

18/5K/7 (Item 4 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

01024716

A MICROPROCESSOR CARD DEFINING A CUSTOM USER INTERFACE
CARTE A MICROPROCESSEUR DEFINISSANT UNE INTERFACE UTILISATEUR PERSONNALISEE

Patent Applicant/Patent Assignee:

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Patent Applicant/Inventor:

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Legal Representative:

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	Country	Number	Kind	Date
Patent	WO	200354787	A1	20030703
Application	WO	2002AU1713		20021218
Priorities	AU	20019660		20011220

Main International Patent Classes (Version 7):

IPC	Level
G06K-019/07	Main

Language Publication Language: English
Filing Language: English
Fulltext word count: 38146

English Abstract:

An electronic card (100) configured to be read by a reading device (300) is disclosed. The card (100) comprising a card portion (270) having a surface (156) onto which are formed a plurality of user interface elements (154) and electronic apparatus (259) attached to the card portion (270). The apparatus (259) comprising a memory (276) in which are retained a plurality of data strings. At least one of the data strings is associated with a corresponding one of the user interface elements (154). The apparatus (259) also comprises a processor means (275) coupled to the memory means (276) and communication means (278) for coupling the processor means (275) to the reading device (300). The processor means (275) is configured to relate reading signals generated from a selection of at least one of the elements (154) and received via the communication means (278) with at least one of the retained data strings. The retained data strings are inaccessible to the reading device (300).

French Abstract:

L'invention concerne une carte electronique (100) configuree pour etre lue par un dispositif de lecture (300). Cette carte (100) comprend une partie carte (270) presentant une surface (156)sur laquelle sont formes une pluralite d'elements d'interface utilisateur

(154) ainsi qu'un appareil electronique (259) relie a ladite partie carte (270). Cet appareil (259) comprend une memoire (276) dans laquelle sont stockees une pluralite de chaines de donnees. Au moins une de ces chaines de donnees est associee a un element correspondant des elements d'interface utilisateur (154). L'appareil (259) comprend en outre un moyen de traitement (275) couple au moyen de memoire (276) ainsi qu'un moyen de communication (278) servant a coupler le moyen de traitement (275) au dispositif de lecture (300). Le moyen de traitement (275) est configure pour etablir un rapport entre des signaux de lecture generes par la selection d'au moins un desdits elements (154) et recus par l'intermediaire du moyen de communication (278), et au moins une des chaines de donnees stockees. Ces chaines de donnees stockees ne sont pas accessibles au dispositif de lecture (300).

Detailed Description:

...by the CPU 275 to determine whether there are valid pass-code entry attempts remaining and if so, whether the entered passcode stored in the **input buffer** matches a predetermined pass-code stored in the storage means 276 of the CPU card 100B. The pass-code checker process will be explained in more detail below with reference to Fig. 32. At sub-step 31 1 1, the data in the data field of the buffer descriptor is **copied** into an output **data**. The process of sub-step 3005 continues at the next sub-step 3113 where the contents of the **working buffer** are copied into the output buffer. At the next sub-stop 3115, the CPU card 100B is set to standard input mode. The process of sub-step 3005 concludes at the next sub-step 3117 where the **input buffer** is cleared.

2 4 Pass-code Checker Process
The pass-code checker process executed at sub-step 3109 of the process of Fig.

18/5K/9 (Item 6 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

00377045

METHOD OF AND SYSTEM FOR PRE-FETCHING INPUT CELLS IN ATM SWITCH
PROCEDE ET SYSTEME DE PRE-APPEL DE CELLULES D'ENTREE DANS UN SELECTEUR ATM

Patent Applicant/Patent Assignee:

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Inventor(s):

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- **BIANCHINI Ronald Jr**

	Country	Number	Kind	Date
Patent	WO	9717788	A1	19970515
Application	WO	96US11850		19960717
Priorities	US	95555021		19951108

Main International Patent Classes (Version 7):

IPC	Level
H04L-012/56	Main

Language Publication Language: English
Filing Language:
Fulltext word count: 5118

English Abstract:

An ATM switch with multicast capability uses a feedback mechanism for resolving contentions. A multicast network reads N cells from an input queue, replicates multicast cells and translates their addresses in accordance with an external look-up table. The processed N cells are stored in a temporary buffer until information regarding the number (F) of cells fed back due to contention in the previous switching cycle is available. A rotator positions N-F cells from the temporary buffer on inputs of an output network so as to assign the cells from the temporary buffer a lower priority than a priority of the feed back cells. The output network selects the cells that can be switched to their destinations and transfers them to output ports. The cells that cannot be switched due to contention are fed back to be presented for the output network consideration in the next switching cycle. At the same time, a pointer of the input queue is decremented by a factor depending on the number of feedback cells, and the number of multicast and unicast cells in the current switching cycle.

French Abstract:

Un selecteur ATM a capacite de destinataires multiples utilise un mecanisme de retour pour regler les problemes d'encombrements. Un reseau a destinataires multiples lit N cellules dans une file d'attente d'entree, reproduit des cellules a destinataires multiples et traduit leurs adresses conformement a une table exterieure. Les N cellules traitees sont stockees dans une memoire tampon temporaire jusqu'a ce que soient disponibles des informations relatives au nombre (F) de cellules retournees en raison de l'encombrement dans le cycle de commutation precedent. Un rotateur positionne N - F cellules, provenant de la memoire tampon temporaire, sur des entrees d'un reseau de sortie, de maniere a attribuer aux cellules provenant de cette memoire une priorite inferieure a celle des

cellules retournees. Le reseau de sortie selectionne les cellules qui peuvent etre commutees vers leurs destinations et il les transfere a des points de connexion de sortie. Les cellules qui ne peuvent pas etre commutees en raison de l'encombrement sont renvoyees pour etre prises en consideration par le reseau de sortie lors du cycle de commutation suivant. En meme temps, un indicateur de la file d'attente d'entree est decremente d'un facteur qui est fonction du nombre de cellules retournees et du nombre de cellules a destinataires multiples ou uniques dans le cycle de commutation en cours.

Claims:

...from said
temporary buffer are supplied at lower inputs of saidoutput network than the rejected packets,
5 The system of claim 2, wherein said **input**
buffer stores a sequence of the received packetsmodified in response to a control signal from saidrotating network.
6 The system of claim 2, wherein said rotating
network comprises a Banyan network.
7 The system of claim 2, wherein said **temporary**
buffer comprises FIFO memories,
8 The system of claim 1, wherein said packets
comprise ATM cells.
9 The system of claim 1. wherein said
distribution network decodes the received **packets** todetect a multicast **packet, replicates** the multicast**packet** to provide a **copy** for each destination of themulticast packet and interacts with an external lookup table to provide the copy with address information.
10 The system of claim 2, wherein said feedback
network comprises a feedback buffer for storing saidrejected packets,
11 In a packet switch having an **input buffer**
coupled to **input** ports, a multicast network coupled tothe **input buffer**, a temporary **buffer** coupled to themulticast network, an output network coupled betweenthe temporary buffer and output ports, and a feedbackpath coupled to the output network...

18/5K/10 (Item 7 from file: 349)
DIALOG(R)File 349: PCT FULLTEXT

00102606

SHARED MEMORY COMPUTER METHOD AND APPARATUS
METHODE ET ORDINATEUR A MEMOIRE PARTAGEE

Patent Applicant/Patent Assignee:

- **SULLIVAN COMPUTER CORP**

Inventor(s):

- **COHN L**
- **SULLIVAN H**

	Country	Number	Kind	Date
Patent	WO	8001421	A1	19800710
Application	WO	80US7		19800107
Priorities	US	792004		19790109

Main International Patent Classes (Version 7):

IPC	Level
G11C-009/06	Main
G06F-15:16	
G06F-03:00	

Language Publication Language: English
Filing Language:
Fulltext word count: 14642

English Abstract:

A shared memory computer method and apparatus having a plurality of sources (S1-Sn, a memory manager (20), and memory units (U1-Um) in which the memory locations of data items are randomly distributed. The memory manager (420) includes a translation module (425) for locating data items in the memory units and a temporary storage buffer (Q1-Qm) for storing at least a portion of messages between sources and the memory units with respect to data items.

French Abstract:

Une methode et un ordinateur a memoire partagee ayant une pluralite de sources (S1-Sn), une gestion de memoire (20), et des unites de memoire (U1-Um) ou les adresses de memoire des donnees elementaires sont distribuees de maniere selective. La gestion de memoire (420) comprend un module de translation (425) pour rechercher les donnees elementaires dans les unites de memoire et un tampon de stockage temporaire (Q1-Qm) pour stocker au moins une partie des messages entre les sources et les unites de memoire par rapport aux donnees elementaires.

Detailed Description:

...to a particular
source by the memor'y manager 620. Other sources of TEST
requests to the same items that have been stored in the

temporary storage buffer are sent status **information** representing failure. If a **copy** of the item was returned by the memory unit this copy is also sent to these other sources.

Note that if the **temporary storage buffer** 630 is full, an **incoming** READ or TEST request may only replace an'old item. The choice of the old item can be made by any of various replacement algorithms... ...from WRITE requests was to be at least as low as then N-n or more different sources would be needed. Now suppose that the **temporary** storagip **buffer** has storage space for just N-n-l data items. if the Opponent repeats a READ reference without having N -1 other requests intervening, a **copy** of the **data** item will still be in the **temporary storage buffer** 630. Therefore, the Opponent is forced (in order to create memory accesses) to plan the referencing patterns so that at least NT, different references are...

NPL abstract files

No relevant results

NPL full-text files

No relevant results